Claims

What is claimed is:

1. A storage device capable of increasing transmission speed, comprising a controller and at least a solid-state storage medium; said controller has an internal system interface that may be connected to an external system end, a microprocessor that processes system instructions, and a memory interface that communicates with said solid-state storage medium; wherein said storage device is featured with: a plurality of data caches is devised between said system interface and said memory interface; said data caches are designed in tiers, wherein the first tier of data cache and the second tier of data cache perform data receiving and transfer alternatively to implement parallel data transmission between said system interface and said memory interface.

2. A storage device capable of increasing transmission speed, mainly comprising a controller and at least a solid-state storage medium; said controller has an internal system interface that may be connected to an external system end, a microprocessor that processes system instructions, and a memory interface that communicates with said solid-state storage medium; wherein said storage device is featured with: a data compression/decompression module with a data compression mechanism is devised in said storage device and is designed to compress the raw data transferred via the system interface at an appropriate compression ratio into

compressed data, in order to increase data access speed.

3. The storage device capable of increasing transmission speed as in claim 2, wherein said data compression/decompression module has an internal decompression mechanism, which is triggered by the microprocessor to decompress the compressed data stored in said solid-state storage medium into original raw data and transfer to the system end.

4. The storage device capable of increasing transmission speed as in claim 2, wherein said storage device has the first data cache, which is wired to said system interface, microprocessor, and data compression/decompression module.

5. The storage device capable of increasing transmission speed as in claim 2, wherein said controller has the second data caches, which is wired to said memory interface, microprocessor, and data compression/decompression module.

6. The storage device capable of increasing transmission speed as in claim 2, wherein said data compression/decompression module is embedded in said controller and between said system interface and said memory interface.

7. A storage device capable of increasing transmission speed, mainly comprising a controller and at least a solid-state storage medium; said controller has an internal system interface that may be connected to an external system end, a microprocessor that processes system instructions, and a memory interface that communicates with said solid-state storage medium; wherein said storage device is featured with:

a data compression/decompression module is devised between

said system interface and said memory interface and is used to compress the raw data transferred via said system interface into compressed data to increase the data transmission speed in said storage device;

a front-end data cache area comprising multi-tiered system-end data caches is devised between said data compression module and said system interface and is designed into a multi-tiered structure; wherein every tier of system-end data cache and its next tier of system-end data cache receive and transfer data alternatively in parallel to implement parallel raw data transmission between said data compression/decompression module and said system interface;

a rear-end data cache area comprising multi-tiered memory data caches is devised between said data compression module and said memory interface and is designed into a multi-tiered structure; wherein every tier of memory data cache and its next tier of memory data cache receive and transfer data alternatively in parallel to implement parallel compression data transmission between said data compression/decompression module and said memory interface.

8. The storage device capable of increasing transmission speed as in claim 7, wherein said data compression/decompression module has a decompression mechanism, which is triggered by the microprocessor to decompress the compressed data in the solid-state storage medium into original raw data and transfer the raw data to the external system end.

9. The storage device capable of increasing transmission speed as in claim 7 or 8, wherein said data

compression/decompression module is embedded in said controller.

10. The storage device capable of increasing transmission speed as in claim 7, wherein the storage capacity of said rear-end data caches is equal to that of the front-end data caches.

11. The storage device capable of increasing transmission speed as in claim 7, wherein said the storage capacity of said rear-end data caches may be smaller than that of the front-end data caches according to the compression ratio.